Vivado Simulator 2017.3

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Running: C:/Xilinx/Vivado/2017.3/bin/unwrapped/win64.o/xelab.exe -wto 84a0f0b44b4c401cbb80523fe79ddc16 --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L secureip --snapshot Testbench\_full\_adder\_behav xil\_defaultlib.Testbench\_full\_adder -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling package std.standard

Compiling package std.textio

Compiling package ieee.std\_logic\_1164

Compiling package ieee.std\_logic\_arith

Compiling package ieee.std\_logic\_unsigned

Compiling architecture behavioural of entity xil\_defaultlib.HALF\_ADDER [half\_adder\_default]

Compiling architecture behavioural\_or of entity xil\_defaultlib.OR\_GATE [or\_gate\_default]

Compiling architecture fa\_arch of entity xil\_defaultlib.full\_adder [full\_adder\_default]

Compiling architecture behavior of entity xil\_defaultlib.testbench\_full\_adder

Built simulation snapshot Testbench\_full\_adder\_behav